



IN2FAB TECHNOLOGY

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## Product Briefing

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OSIRIS™

Optimal Scaling IP Reuse Integration System

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# Rapid Analog Porting

Process to Process





Geometry to Geometry

**OSIRIS** is the industry's leading capability for the rapid porting of analog and custom intellectual property (IP) from any Foundry/Process/Geometry to any Foundry/Process/Geometry. With extensive silicon success across all CMOS geometry nodes down to and including 90nm, BiCMOS and SiGe, OSIRIS is widely tested and proven. Design cycle time improvements of up to 10X compared to redesign using traditional custom design methods have regularly been realized.

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## KEY FEATURES

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-  **10X Faster**
-  **10M Transistors**
-  **Topologically exact**
-  **EDA Interoperable**

## Key Features and Benefits

- Rapid porting of analog and custom IP such as ADCs, DACs, PLLs and RISC microprocessors and microcontrollers made possible in days
- Limitless design size can be ported with up to 10M transistors previously processed
- Topology and hierarchy exactly replicated in the porting methodology meaning design intent is preserved, critical for analog performance
- Full support for Process Development Kits and parameterized cells (pcells)
- Full interoperability and integration with Cadence Design Systems' Design Framework II™ environment



## Analog/Custom Design Challenge

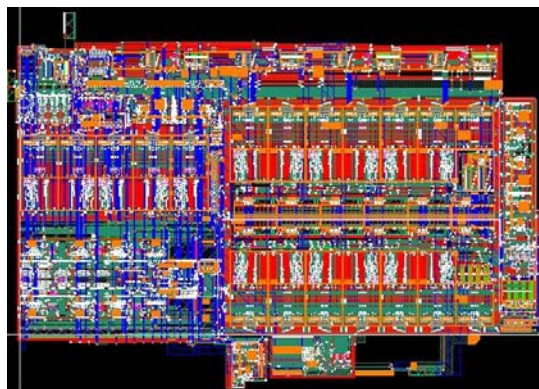
The predicted growth in analog as a function of designs containing analog circuitry is forecast to increase from around 30% in 2003 to greater than 70% in 2006. As a percentage of die area dedicated to analog within the industry this is growing from 10% in 2003 to 15% by 2008. In SoC and ASSP development terms both the need for proven analog IP and the design overhead associated producing it will increasingly become the critical design factor. This means:

- **More resources are required delivering greater productivity – the need for automation improvement is unavoidable**
- **Reuse through portability rather than recreation of analog IP to improve time to market is a critical**
- **Reuse of proven hardened IP to improve design quality by using known design structures is vital**

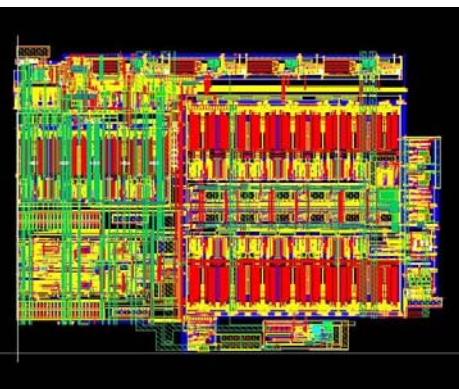
## OSIRIS

Using the patented technique of “Complex Nodal Scaling” OSIRIS provides a breakthrough technology enabling previously proven analog IP to rapidly be ported between different processes and geometries reducing design cycle time, improving design quality and reducing risk.

**Origin**



**Target**

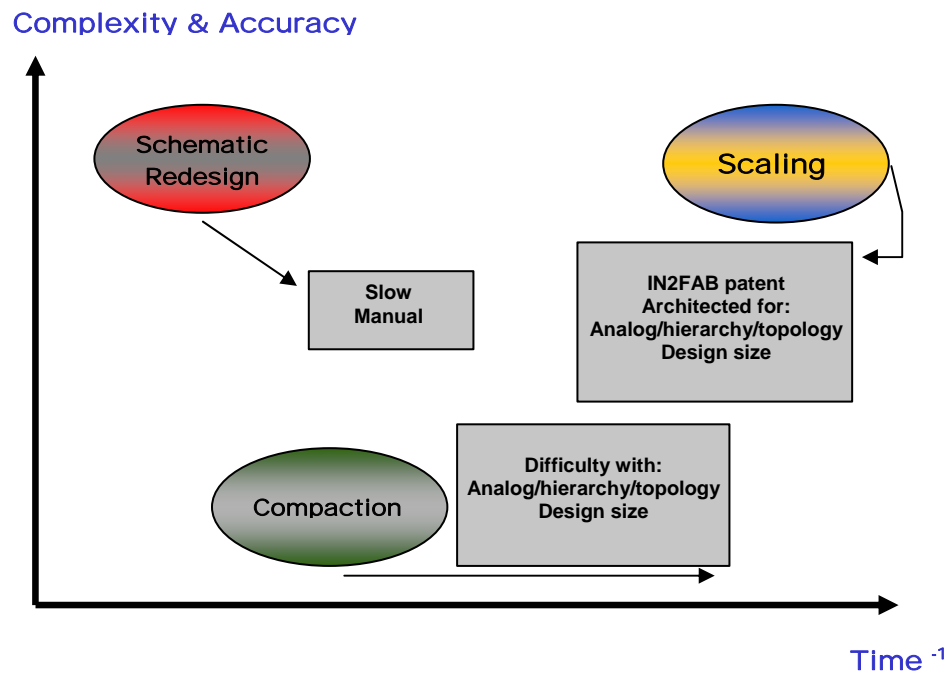


IF section from a communications device retargeted from an IDM process to an external foundry including a geometry change. Overall chip port took 6 weeks

## Analog Reuse Options

Comparing the three accepted methods for analog reuse and physical porting yields some interesting conclusions as shown graphically below:

- Schematic based redesign is still the most widely adopted practice in the industry despite punitive manual re-layout overhead meaning automated approaches to this point have not delivered an effective solution
- Compaction tools have consistently struggled to handle design complexity and by their very nature undermine the essence of an analog circuit – its topology. As a result only minimal improvements in cycle time can be gained with the high penalty trade-off of being able to handle only small circuits.
- Conversely the technique of scaling for which IN2FAB has the patent rights enables analog circuits to be ported to an optimal die size, maintaining topology and hierarchy for any design size. The accuracy and performance of the analog circuitry is preserved through design right by construction.

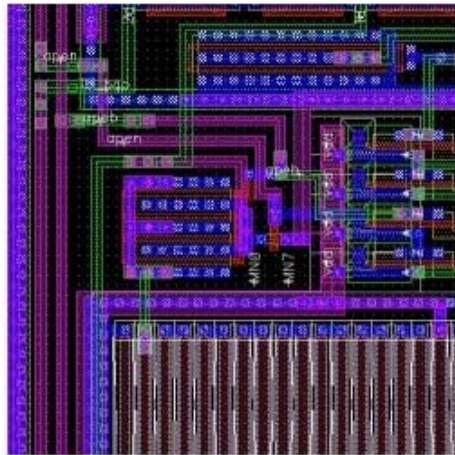


OSIRIS scaling methodology delivers high quality analog porting faster

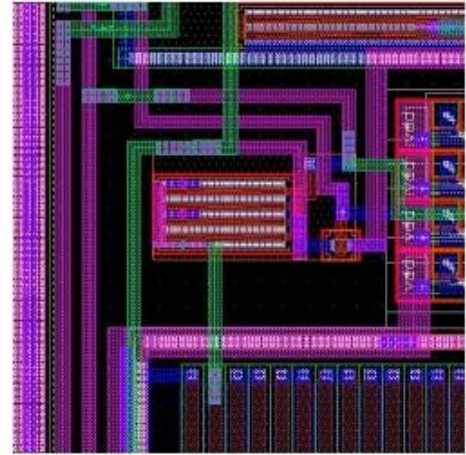
## OSIRIS Flow Overview

IN2FAB's OSIRIS system uses a patented technique called "complex nodal scaling" to move designs between processes and geometries. After calculating the relationships between the old and new processes, the layout is mapped to the new layers and component types then scaled to an optimum size, completely preserving the hierarchy and topology. This new layout is then adjusted through a series of powerful manipulation routines to remove DRC violations and adjust component values to meet performance requirements.

Working within the Cadence design framework, the OSIRIS tools provide the user with flexibility to modify the design at any stage of the migration process and make structural changes to their layout while OSIRIS takes care of data processing and shape based violations. The benefit of this approach is that designs of any size can be handled and the original intent of the designer is carried forward into the ported design.



**0.13µm**



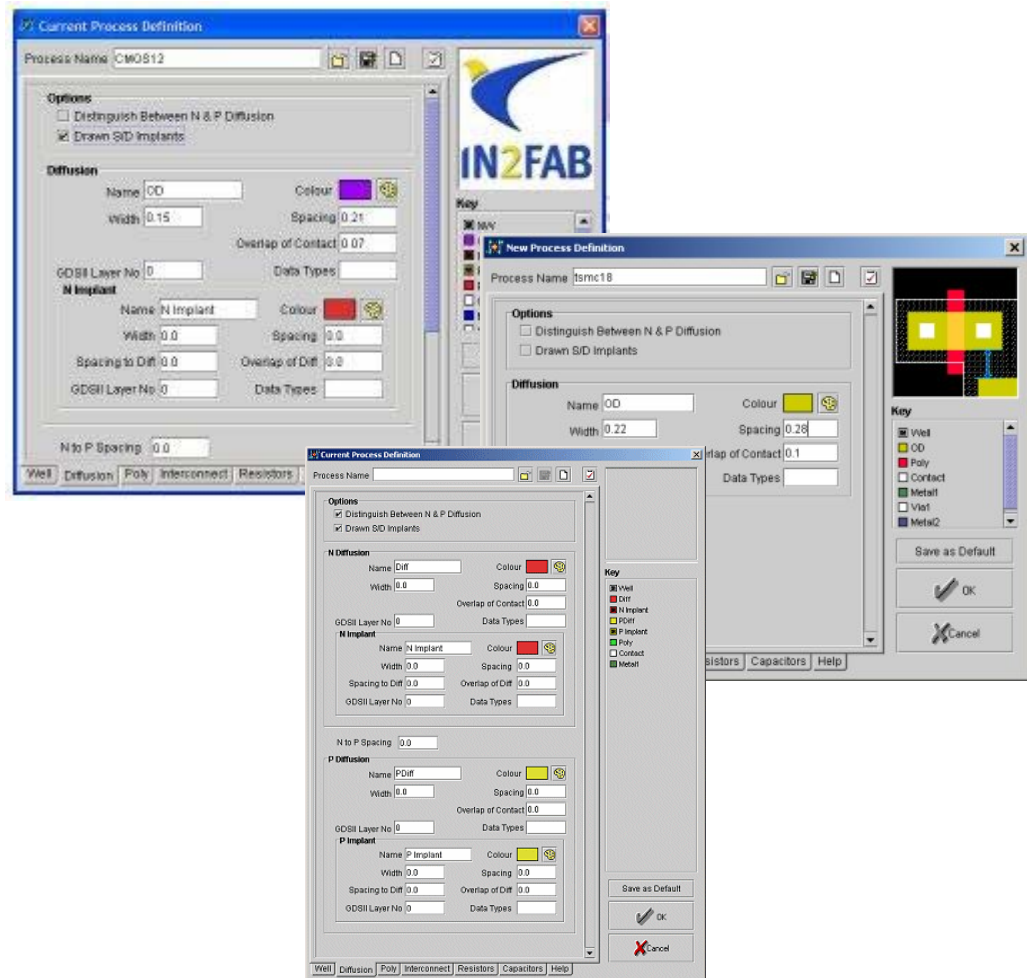
**90nm**

The OSIRIS user interface automatically finds layers, symbolic devices and parameterized cells and allows easy mapping between the old manufacturing process and the new. Design data is mapped automatically or by user selection ensuring an easy transfer of data from one process to the next.

The new layout matches the old in topology and hierarchy, preserving critical circuit balance without a lengthy set-up process or the overhead of the user having to generate design constraints.

## Process & Design Analysis

The initial task involves analyzing the circuit along with the source and target design rules in order to determine the optimum size for the device in the new manufacturing process. Once this is complete, this provides all the information necessary for the layout to be scaled to the new size and modified to meet the constraints of the new manufacturing process design rules. The new die size for the design in the new rules is precisely known up front.



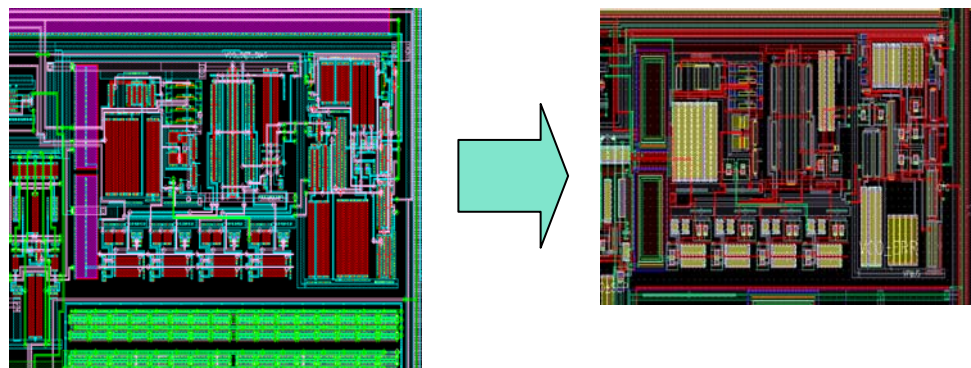
IN2FAB's Java based Process Analyzer tool allows designers to understand the impact of various target manufacturing process rules on their circuit.



## Maintaining Analog Performance

OSIRIS can be used for any geometry size and can cope with widely differing foundry styles such as extra implants and wells. The system is fully hierarchical and preserves the integrity of the original design by matching the topology and intent of the original design layout into which has gone considerable design effort.

Critical signals and device matching are maintained throughout the process without the need for intervention from the designer. Extra layers may be added and redundant layers removed giving complete foundry independence. Full control over power net sizing and via stacks is user definable and maintainable. The OSIRIS system is fully hierarchical and preserves both the hierarchy and topology of the original circuit, ensuring critical matching and wire positions are retained and layout intent preserved.



**VCO section from a wireless device retargeted between IDM processes involving a geometry change. Overall chip port took 7 weeks including RF**

In analog designs, especially important is the ability to maintain exact physical or topological relationships. In this way the work of the original designer to ensure correct balancing and matching is exactly maintained. The fundamental principle behind the success that OSIRIS can bring is to create design right by construction. Because of this the first time success rate is always high for the ported design.

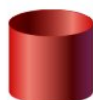
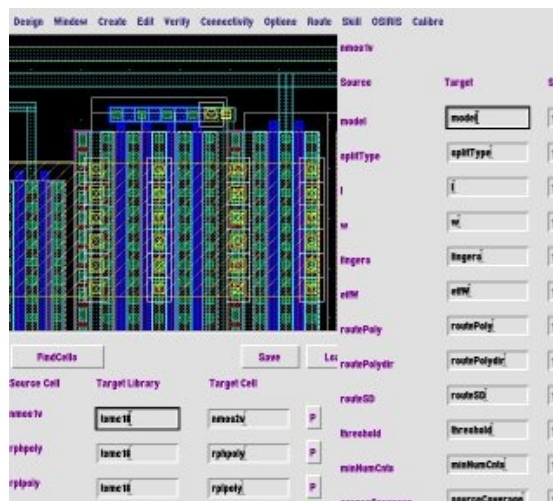
Working within the Cadence Design Framework IIT<sup>TM</sup> environment means that full maintainability and user control over the design both during the port and subsequently is ensured. OSIRIS is the vehicle to get to analog design completion rapidly.

## Process Design Kits & Parameterized Cells

Many analog layouts are constructed using parameterized cells and symbolic vias from foundry process design kits (PDKs). OSIRIS features an advanced user interface that automatically finds component values and gives users an easy method of mapping device types and parameters from one process to the next. Using parameterized cells from the target foundry guarantees devices are correct by construction and match the foundry's design criteria.

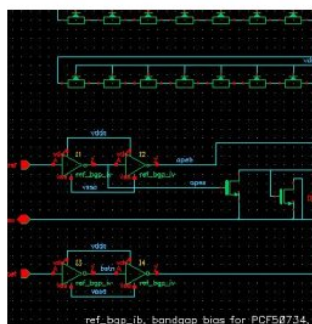
Parameterized cells from the source design are matched to those in the target process through a simple user interface.

Component overlaps and connections are adjusted automatically to correct differences in target device shape and construction.



PDK

### OSIRIS PDK Migration



Schematic translation & CDF

Layer mapping

Basic layout elements

- Polygons, paths, text, instance, mosaic

Advanced layout elements

- Symbolics, P-Cells, net data

GUI driven parameter mapping

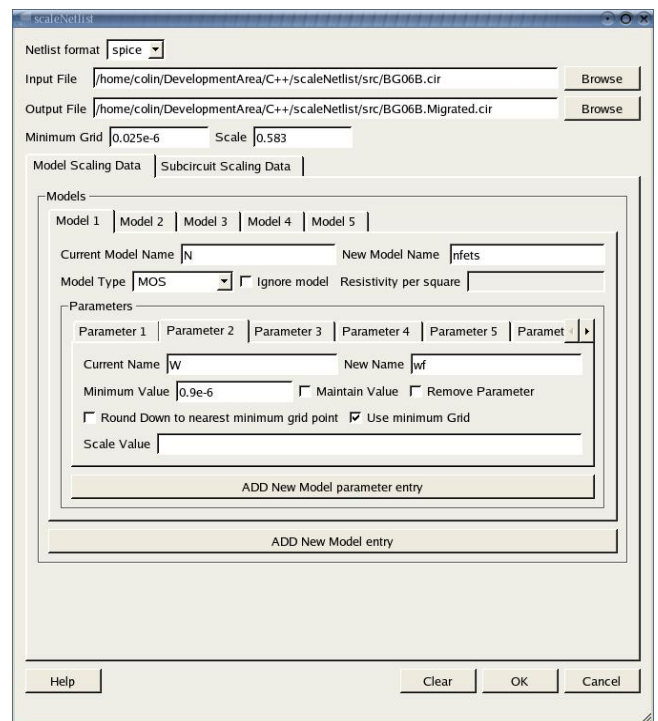
## Netlist Retargeting

In addition to physical design migration, OSIRIS features a fully configured tool option for netlist translation. The tool suite supports transistor and gate level netlists with facilities for component, model and parameter mapping. At a very early stage the retargeted netlist is available to support other design work such as simulation.

The tools can translate Spice, cdl and also has provision for other conversions such as Spice to Verilog and Verilog to Spice.

A number of features and utilities are available to enable the user to specify requirements at the model or parameter level including:

- Parameter scaling including equations with user control
- Parameter scaling to a grid
- Non-scaling of parameters
- Parameter name change
- Parameter removal from model
- Parameter addition to a model
- Sub-circuit removal or replacement
- Sub-circuit renaming

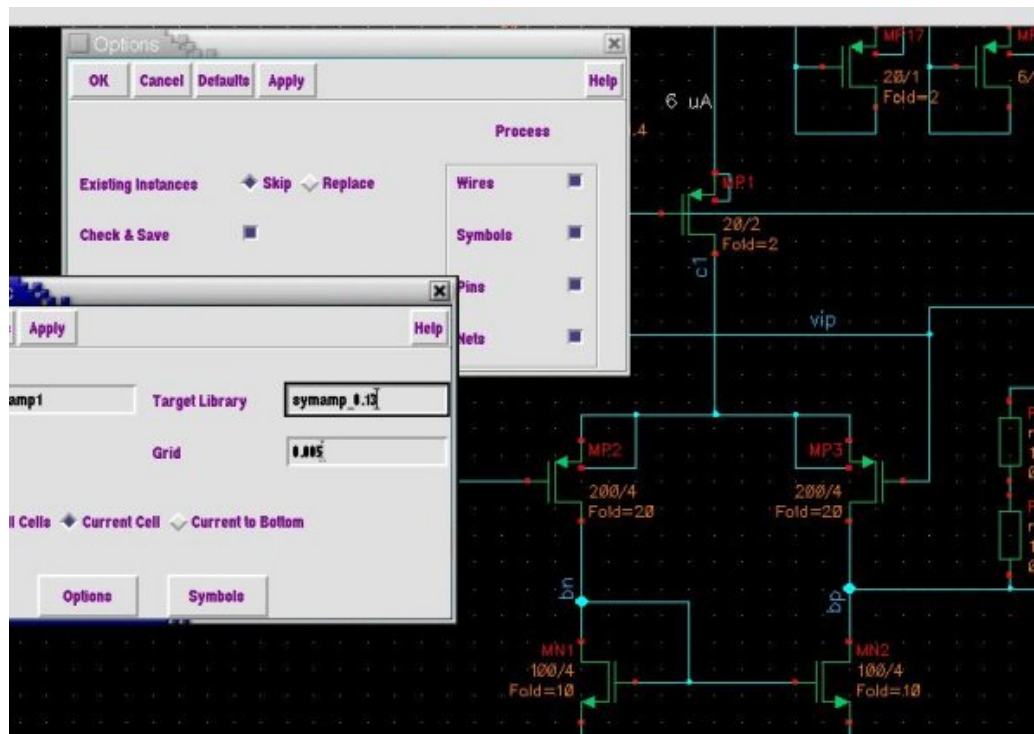


The netlist translation tools are self-contained and can be run externally to the Cadence environment. All are available for Solaris and Linux.

## Schematic Retargeting

OSIRIS contains schematic migration tools which translate the physical and model information from a source schematic cell view to any new process or library. Working within Cadence's Design Framework II™ environment enables the OSIRIS process porting tools to update model and symbol information while retaining the structure and hierarchy of the user's original schematics.

Component description data is automatically retrieved from the foundry process design kit and presented to the user through a simple user interface to allow scaling and mapping of component connections, parameters and values.



## Product Specifications

### Functionality

- Fully hierarchical top down analog and custom porting tool suite with faithful topology preservation
- Design rule analysis and comparison
- Support for Process Design Kits & parameterized cells
- Intelligent database including preservation of paths and multi part paths, Symbolics, connectivity and device properties
- Fully integrated within Cadence Design Framework II™
- Schematic and netlist porting
- No limit on design complexity, size or differences between origin and target design rules

### Input Files

- GDSII
- Cadence CDBA
- SPICE and CDL netlist
- Cadence Schematic
- OpenAccess
- Foundry Process Design Kit
- Standard Cell Library

### Output Files

- GDSII
- Cadence CDBA
- SPICE and CDL netlist
- Cadence Schematic
- OpenAccess

### Platform & OS

- Sun Solaris
- Linux

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